AUG. 12. 2004 4:52PM BST&Z - CM

Appl. No. 09/334,693 Amdt, dated 08/12/2004 Reply to Office action of 05/12/2004

REMARKS

This Amendment is in response to the Office Action mailed 05/12/2004. In the Office Action, the Examiner rejected claims 1-21 and 23-44 under 35 U.S.C. § 102. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Rejection Under 35 U.S.C. § 102

2. The Examiner rejects claims 1-21 and 23-44 under 35 U.S.C. § 102(e) as being anticipated by Parry et al. (US 5,822,381).

Applicant has cancelled all outstanding claims 1-21 and 23-44 and now presents new claims 45-74 that claim substantially the same subject matter in a form that more clearly distinguishes the claimed invention from the prior art. For the convenience of the Examiner, applicant will point out the similarities of the present claims to the cancelled claims. However, it is intended that the newly presented claims be examined on their own merits. The scope of the newly presented claims is not limited by any similarities to or difference from the previously presented claims.

Regarding claim 45, this claim includes elements previously presented in claims 1 and 5-10. The Examiner asserts that Parry discloses each and every element of previously presented claims 1 and 5-10. Applicant respectfully disagrees and submits that the distinctions of the present invention from the disclosure of Parry will be more clear in newly presented claim 45.

The Examiner cites the filter circuit and sampling window of Parry as disclosing the switching between a synchronization state and an alarm state. New claim 45 claims maintaining a locked state when a predefined number of local clock cycles generated by the local clock generating circuit is observed between successive occurrences of a global synchronization signal provided to each of the plurality of components of the distributed system. This is distinct from Docket No: 81862,P116

Page 15 of 17

JAH/phs

Appl. No. 09/334,693 Amdt. dated 08/12/2004 Reply to Office action of 05/12/2004

the filter circuit and window of Parry because Parry does not require that a predefined number of local clock cycles be observed to maintain a state. Rather Parry allows for a window in which some variation of the number of clock cycles is permitted before there is a change of state.

Parry discloses only a normal and a fail state. Parry discloses generating a global clock fail signal when a predetermined number global clocks occur outside the filter window without the intervening occurrence of the edge of the global clock signal within the filter window. Col. 7, lines 52-63. The distinct difference of the present invention is apparent from the claimed short and long states which have no counterpart in Parry. The present invention can enter the alarm state from the short or the long state if a second difference in the number of local clock cycles is observed. Thus, the present invention provides for a transition to the alarm state even when intervening edges of the global clock are observed at the expected time. This is in great contrast to Parry which discloses that the global clock fail signal is generated only if a predetermined number of missed edges have occurred without the intervening occurrence of an edge. Col. 7, lines 59-63.

Regarding claims 51, 57, 63, and 69, these claims are similar to claim 45. They are distinguished from the disclosure of Parry for the same reasons discussed above for claim 45.

Regarding claim 46, this claim includes elements previously presented in claim 2. The Examiner does not specifically cite the portions of Parry alleged to disclose the claimed element of "the local clock generating circuit enters the synchronization state only after observing a predetermined number of occurrences of successive local clock cycles between the successive occurrences of the global synchronization signal" of claim 2. Applicant respectfully submits that col. 8, line 38, through col. 9, line 24, of Parry are the only disclosure of initialization of the clock system. Parry discloses disabling the global clock signal, setting the local clock circuits to

Docket No: 81862,P116

AUG. 12. 2004 4:53PM

BST&Z - CM

Appl. No. 09/334,693 Amdt. dated 08/12/2004

Reply to Office action of 05/12/2004

an initialization state, and then enabling the global clock signal. The first received edge of the global clock signal following this procedure starts the local counters counting in synchronization. Col. 9, lines 21-23. This is entirely unlike the claimed element of claim 46 of "observing the predefined number of local clock cycles between a second predefined number of successive occurrences of the global synchronization signal and then entering the locked state."

Regarding claims 52, 58, 64, and 70, these claims are similar to claim 46. They are distinguished from the disclosure of Parry for the same reasons discussed above for claim 46.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-21 and 23-44 under 35 U.S.C. § 102(e) as being anticipated by Parry and not apply this rejection to newly presented claims 45-74.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY JOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 08/12/2004

James Henry

Reg. No. 41,064

Tel.: (714) 557-3800 (Pacific Coast)